Register No : _____

THE KAVERY ENGINEERING COLLEGE

(An Autonomous Institution)

UG/PG DEGREE END SEMESTER THEORY EXAMINATIONS, APRIL-MAY 2026

Second Semester

Master of Computer Application

PMCVA103 - INTRODUCTION TO COMPUTER ORGANIZATION AND OPERATING SYSTEMS

Regulations - 2024

Duration: 3 Hrs. ***Maximum: 100 Marks***

PART – A (ANSWER ALL QUESTIONS) (Marks 10*2=20)

Q.No	*Questions*	*BLT*	*CO*	*Marks*
1.	What are the basic steps required to execute an instruction by the processor?	L1	1	2
2.	Write down the basic performance equation.	L1	1	2
3.	Illustrate stalls in the context of pipelining?	L1	2	2
4.	What do you mean by delayed branching?	L2	2	2
5.	What is MMU? Mention the components of MMU.	L2	3	2
6.	Why IO devices cannot be directly be connected to the system bus?	L2	3	2
7.	Why is the Operating System viewed as a resource allocator and control program?	L2	4	2
8.	Draw the process state transition diagram.	L1	4	2
9.	Show that mutual exclusion may be violated if the signal and wait operations are not executed atomically.	L2	5	2
10.	If Round Robin is used with a time quantum of 1 second, the turnaround time for Process 2 will be,	L2	5	2

Process No CPU Time	Process No CPU Time
P1	1 hour
P2	1 second
P3	1 minute

PART – B (ANSWER ALL QUESTIONS) (Marks 5*16 = 80)

Q.No			*Questions*	*BLT*	*CO*	*Marks*
11.	a	i	Discuss in detail about the basic Operational concept of instruction execution with neat Diagram.	L3	1	8
		ii	Illustrate the following sequence of instructions and identify the addressing modes used. Also, explain the operation done and effective address calculation for every instruction. • Move R0, R5 • Add (R5)+, R0 • Move (R0), R5 • Move #200, R0	L3	1	8
			Or			
	b	i	Registers R1 and R2 of a computer contain the values 1200 and 4600. Identify the addressing mode used and calculate the effective address	L2	1	8

(EA) of the memory operand in each of the following instructions.

- Load 20(R1), R5
- Move #3000, R5
- Add -(R2), R5
- Subtract (R1)+, R5

	ii	How the location of operands can be specified in a machine instruction and explain how the information within the address field is interpreted? Discuss how the actual or effective address of the data needed is computed with example.	L2	1	8
12.	a	Consider a processor is having single bus organization of the Datapath inside a processor. Write the sequence of control steps required for each of the following instructions: a) Add the immediate number (NUM) to register R1. b) Add the contents of memory location NUM to register R1. [Add (NUM), R1].	L3	2	16
		Or			
	b	Consider a processor having single bus organization for the datapath inside a processor. Write and explain the sequence of control steps required for executing the instruction for storing the contents of memory location to register.	L3	2	16
13.	a	i Illustrate the structure of semiconductor RAM memories. Discuss the read and write operations in detail.	L1	3	8
		ii Explain about the basic cell of an associative memory along with its operation and show how associative memories can be constructed using this basic cell.	L1	3	8
		Or			
	b	Discuss about the use of cache memories? Discuss the possible methods of specifying where memory blocks are placed in the cache using mapping functions.	L1	3	16
14.	a	How a user program can interface with the operating system? What will be invoked by the OS in order to serve the user request? Explain the purpose and importance of such invocation and Differentiate user-level threads and kernel-level threads.	L2	4	16
		Or			
	b	Some computer systems do not provide a privileged mode of operation in hardware. How is it possible to construct a secure operating system for these computer systems?	L2	4	16
15.	a	What do you mean by a binary semaphore and a counting semaphore? Along with the necessary 'C'-struct, explain the implementation of wait() and signal() semaphore operations and develop pseudo to implement.	L3	5	16
		Or			
	b	Develop pseudo code to implement its operations and show how wait() and signal() semaphore operations could be implemented in multiprocessor environments the Test and Set instructions.	L3	5	16

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